CLAIMS

WHAT IS CLAIMED IS:

5   1.   A phase locked loop (PLL) circuit for a fractional frequency

division synthesizer, comprising:

a voltage controlled oscillator (VCO) for generating an output signal of

a frequency proportional to a predetermined frequency control voltage, and for

generating a clock signal delayed by a time period corresponding to a

10   fractional division control data signal;

an integer division logic circuit for generating a feedback signal by

dividing the delayed clock signal supplied by the VCO in response to an

external integer division ratio data and a predetermined division ratio;

a phase comparator for detecting a phase error between an input signal

15   and the feedback signal, and for generating a phase error signal corresponding

to the phase error;

a charge pump circuit for generating a charge pump output current

corresponding to the phase error signal; and

a loop filter for converting the charge pump output current to the

20   frequency control voltage.

2.   The circuit of claim 1, wherein said delayed clock signal

generated from the VCO is formed of a fraction of the clock signal.

3.   The circuit of claim 2, wherein said VCO comprises:

an oscillator for generating an output signal of a frequency in proportion to the frequency control voltage, and for generating 2^Y delay

5   signals (where Y is a positive integer) delayed by a predetermined time with respect to the output signal; and

a switching circuit for generating the delayed clock signal from one of the 2^Y delay signals in response to the fractional division control data.

10   4.   The circuit of claim 3, wherein the delay signals have delay times that are equal, and the sum of delay times of the delay signals is equal to a cycle of the output signal.

5.   The circuit of claim 3, wherein only one of said 2^Y fractional

15   division control data bits has a value of logic '1' exclusively.

6.   The circuit of claim 5, wherein said switching circuit is composed of 2^Y switches respectively corresponding to the delay signals generated from the oscillator, where each switch is controlled by the

20   corresponding fractional division control data bit, and transmits the delay signal generated from the oscillator to the delayed clock signal.

7.   The circuit of claim 3, wherein said fractional division ratio data comprises X bits (where X is a positive integer).

8.   The circuit of claim 7, wherein said fractional division control logic circuit comprises:

a second counter for performing a counting operation in synchronous response to the feedback signal, for comparing an internal count value with a higher (X–Y) bit of the fractional division ratio data, resulting in generation of a second control signal;

a third counter for performing counting operations a number of times corresponding to a value of the sum of the second control signal and a lower Y bit of the fractional division ratio data, and thereby generating a count value;

a decoder for generating a decoding data from the count value of the third counter; and

a latch circuit for generating, in synchronous response to the delayed clock signal, the fractional division control data from the decoding data.

9.   The circuit of claim 7, wherein said second counter generates the second control signal at a value of logic '1' if the internal count value is lower than the higher (X–Y) bit of the fractional division ratio data, and for generating the second control signal at a value of logic '0' if the internal count value is equal to or greater than the higher (X–Y) bit.

10.   The circuit of claim 2, wherein said integer division logic circuit, comprises:

a dual modulus prescaler for selecting one of predetermined plural division ratios in response to a first control signal, for dividing the clock

5   signal divided by the selected division ratio, and for generating a first division signal;

a frequency divider for dividing the first division signal in response to the integer division ratio data, and for generating the feedback signal; and

a first counter for performing counting operations in synchronous

10   response to the feedback signal, for comparing the internal count value with a critical value supplied from external sources, and thereby generating the first control signal.

11.   The circuit of claim 10, wherein said first counter generates the

15   first control signal having logic '1' if the internal count value is lower than the critical value supplied from external sources, and generates the first control signal having logic '0' if the internal count value is equal to or greater than the critical value.

20   12.   The circuit of claim 11, wherein said first counter is formed of a swallow counter.

13.   The circuit of claim 7, wherein said fractional division control

logic circuit comprises:

a second counter for performing a counting operation in synchronous

response to the feedback signal, for comparing an internal count value with a

5   higher (X–Y) bit of the fractional division ratio data, resulting in generation of

a second control signal;

a third counter for performing counting operations as many as times as

a sum of the second control signal and a lower Y bits of the fractional division

ratio data in synchronous response to the first division signal, and thereby

10   generating a count value;

a decoder for generating a decoding data from the third counter; and

a latch circuit for generates the fractional division control data from the

decoding data in synchronous response to the delayed clock signal.

14.   The circuit of claim 13, wherein said second counter generates

15   the second control signal of logic value '1' if the internal count value is lower

than the higher (X-Y) bit of the fractional division ratio data, and generates

the second control signal of logic value '0' if the internal count value is equal

to or greater than the higher (X-Y) bit.

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15. The circuit of claim 10, wherein said fractional division control

logic circuit comprises:

a second counter for performing a counting operation in synchronous

response to the feedback signal, for comparing an internal count value with a

5 higher (X–Y) bit of the fractional division ratio data, resulting in generation of

a second control signal;

a third counter for performing counting operations as many as times as

a sum of the second control signal and a lower Y bits of the fractional division

ratio data in synchronous response to the first division signal, and thereby

10 generating a count value;

a decoder for generating a decoding data from the third counter; and

a latch circuit for generates the fractional division control data from the

decoding data in synchronous response to the delayed clock signal.

16. The circuit of claim 15, wherein said second counter generates

15 the second control signal of logic '1' if the internal count value is lower than

the higher (X-Y) bit of the fractional division ratio data, and generates the

second control signal of logic '0' if the internal count value is equal to or

greater than the higher (X-Y) bit.

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